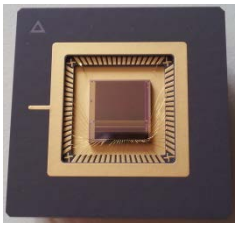

SCI640D

General Description

SCI640D is a Readout Integrated Circuit (ROIC) for detector arrays with a resolution of 640x512 pixels and a pitch of 10µm. It provides up to 190 frames per sec through 1 high speed digital LVDS output port. It has on-chip 16-bit ADCs. Total power dissipation of the ROIC is 200mW. The pixel is based on a Capacitance Trans-Impedance Amplifier (CTIA) offering a maximum full well capacitance of 250ke$^-$ and exposure time is controlled globally through an electronic snapshot shutter. Column parallel pre-amplifiers buffer the analog signal from the pixel into 16bit column parallel ADCs. Many different operating modes and conditions can be programmed via serial interface. Important features that can be changed are: full well capacity (FWC); snapshot shutter mode, i.e. Integrate Then Read (ITR), Integrate While Read (IWR) and Non-Destructive Read (NDR), column amplifier gain. All biases are generated on-chip and derived from one common band-gap reference. These biases can be programmed via the serial interface to optimize power dissipation and full well capacitance for each operating mode. Most sub-blocks can be tested and calibrated individually, i.e.: column amplifier, ADC, high-speed output port. The exposure time and readout are controlled by the three signals “exp”, “frame” and “line”. The array readout directions are: vertically – bottom to top, horizontally – center to outside. Regions of Interest are defined by the “line” pulse in the horizontal dimension. Vertical ROI windowing can be achieved by fast clocking through multiple lines with a frequency as fast as the pixel clock. The ROIC supports readout of detectors of both polarities but is optimized for P diodes on N material. Minimum integration time is 10usec.

Features

An overview of the SCI640D specifications is given in Table 1. The listed parameters are representative for an average device. Individual ROIC performance may slightly deviate.

Parameter	Value
Array Size	640x512
Pixel pitch	10 µm
Detector polarity	P or N
Die Size	7.8 x 8.2 mm^2
Exposure time control	Snapshot shutter: ITR, IWR, NDR
Integration time jitter	< 100nsec
Latency (after trigger)	< 100nsec
Charge capacity	programmable
minimum	18 k e$^-$ (high gain)
maximum	250 k e$^-$ (low gain)
Input Referred Noise	
High gain mode	25 e$^-$ (high gain)
Low gain mode	110 e$^-$ (low gain)
Integration time range	10 µs – 30 ms
Frame rate	120 Hz(programmable up to 190Hz)
Output	Digital, LVDS, 16-bit
Output format	Raw, un-encoded bit stream
Output data rate	up to 1 Gbit/sec
Number of Output channels	1
Master Clock	up to 250 MHz
Power	3.3V/1.8V
Logic I/O levels	0.0V/3.3V
Serial Interface	Yes(single long word)

Table 1: SCI640D datasheet