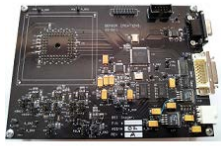

CPLD Board

General Description

The CPLD Board here consists of a programmable logic device, ADCs, DACs, voltage regulators to provide programmability and flexibility in controlling SCI designed Image Sensor. The board here can be programmed to provide appropriate control signals to the Image sensor. This board can be used for testing the image sensor as well as to create an image from the sensor in place. The board can be controlled from a computer using RS232 serial connection. It also consists of a GUI for adjusting voltages and currents. The JTAG connector helps you to create, modify and also test the board along with the sensor. The board presented here is manufactured in a 5 layer process presenting less clutter to the end user. It consists of voltage regulators to provide a constant voltage to all the chips on board. It consists of a camera link interface to produce an image from the sensor in place on the board.

Features

An overview of the CPLD Board specifications is given in Table 1. The listed parameters are representative for the CPLD board in place.

Parameter	Value
Board Size	5x7 sq. inches
Plugin socket	Zero insertion socket(holds the sensor)
Voltage Regulators	5V to 3.3V fixed voltages
Adjustable output	3.8V to 14V
Shutdown(Iq)	16µA
Power Supply voltages	12V
ADCs	14-bit, low power
DNL	+/- 0.7 LSB
SNR	>73dBc
Supply	5V analog, 3.3V/5V driver supply
DACs	8-bit voltage output (quad voltage outputs)
Supply	+15V
Error	+/- 1LSB
Data Load time	50ns
JTAG	10 pin connector
Camera Link Interface	2-bit channel Link – 66MHz
Supply	3.3V
Bandwidth	231 MBps
Common mode range	+1V
CPLD	LCMXo2280C
Vcc voltage	1.2/1.8/2.5/3.3 V
I/O Banks	8

Table 1: CPLD Board datasheet